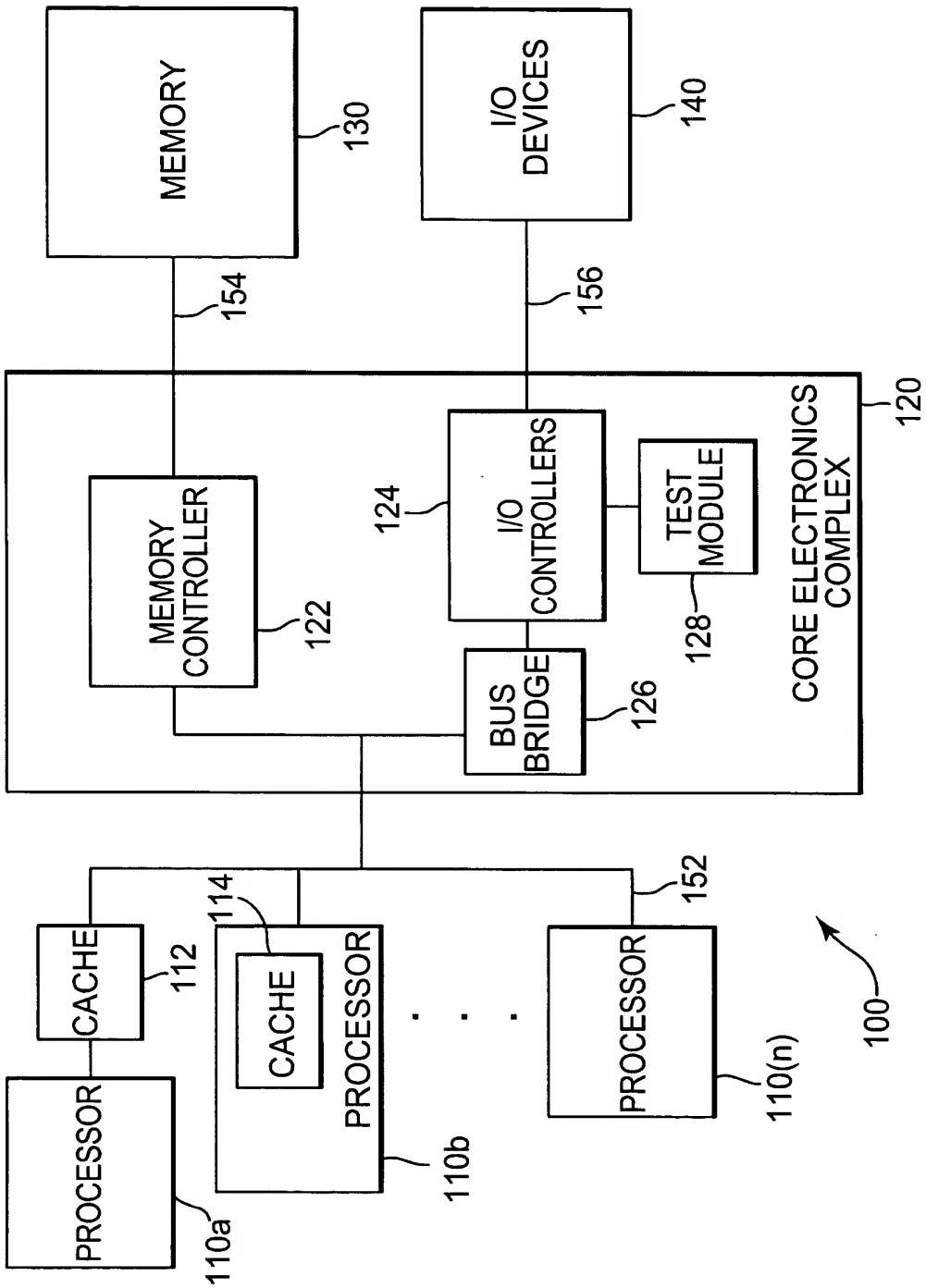
MEMORY
130
I/O DEVICES
140
154
156
MEMORY CONTROLLER
122
124
I/O CONTROLLERS
TEST MODULE
128
BUS BRIDGE
126
CORE ELECTRONICS COMPLEX
120
152
114
CACHE
112
CACHE
PROCESSOR
110b
PROCESSOR
110(n)
PROCESSOR
110a
100

Fig. 1

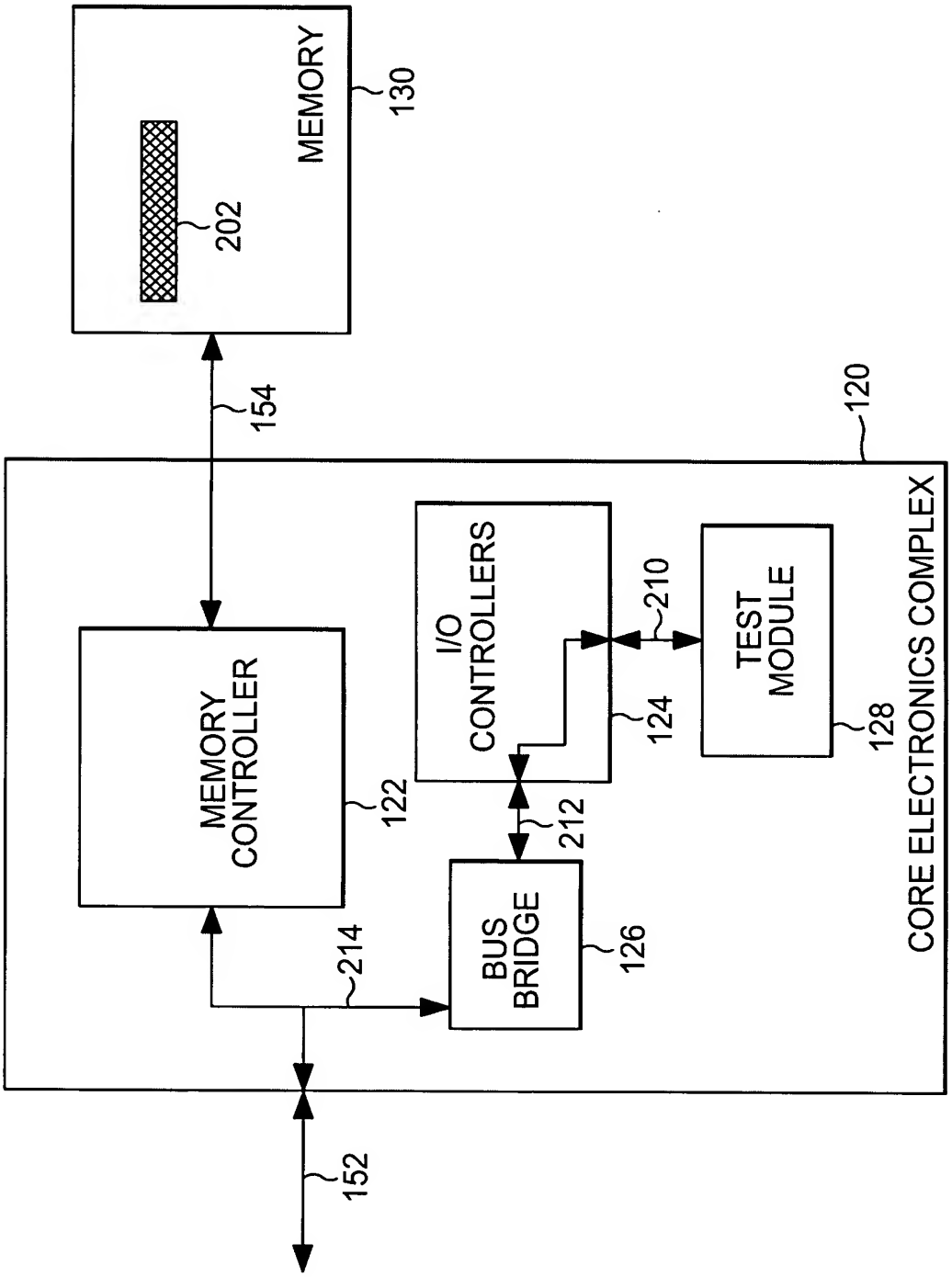
MEMORY
130
202
154
120
MEMORY CONTROLLER
122
I/O CONTROLLERS
210
TEST MODULE
124
128
212
BUS BRIDGE
126
214
CORE ELECTRONICS COMPLEX
152

Fig. 2

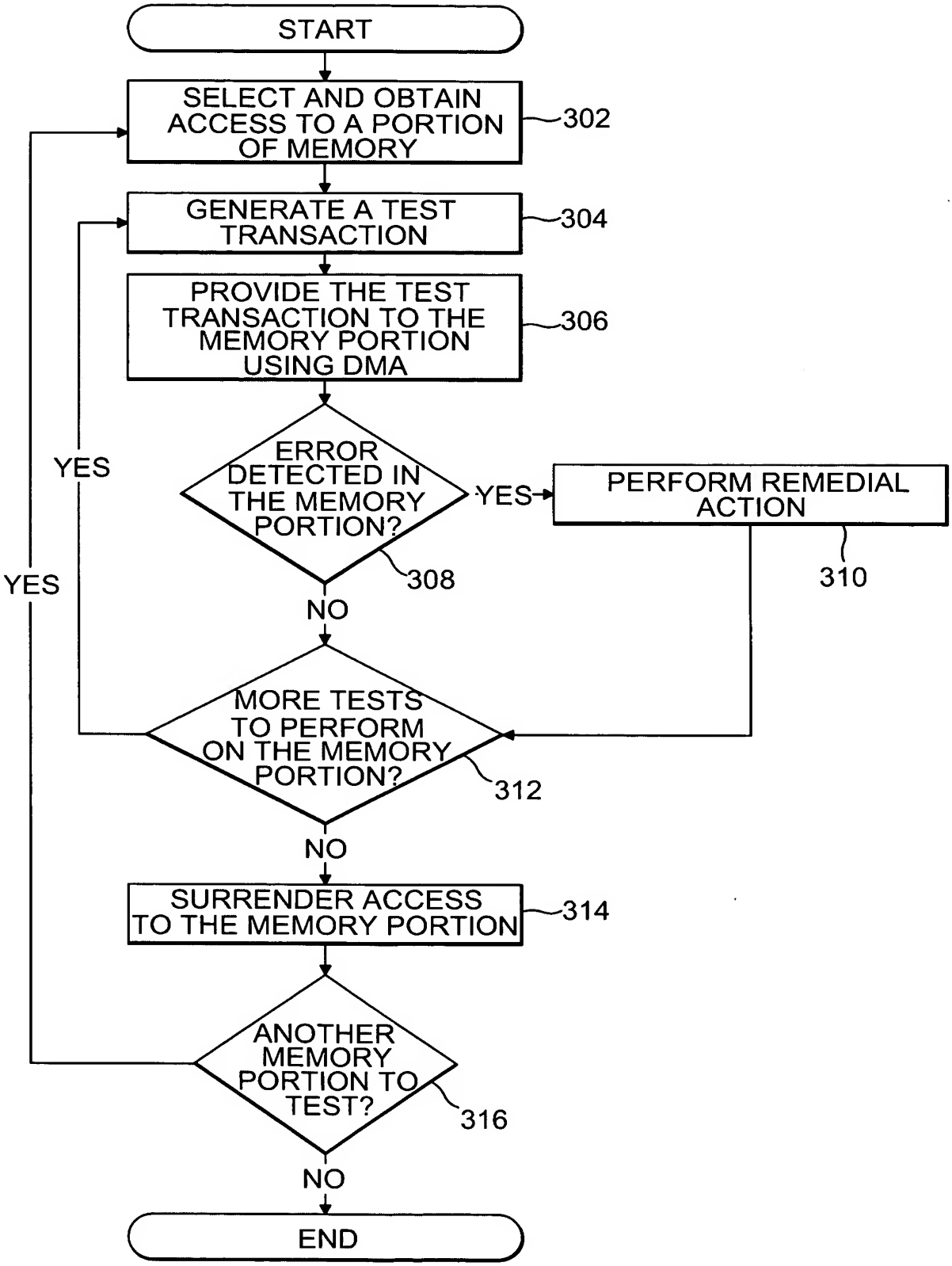
START
SELECT AND OBTAIN ACCESS TO A PORTION OF MEMORY
302
GENERATE A TEST TRANSACTION
304
PROVIDE THE TEST TRANSACTION TO THE MEMORY PORTION USING DMA
306
ERROR DETECTED IN THE MEMORY PORTION?
308
YES
PERFORM REMEDIAL ACTION
310
NO
MORE TESTS TO PERFORM ON THE MEMORY PORTION?
312
YES
NO
SURRENDER ACCESS TO THE MEMORY PORTION
314
ANOTHER MEMORY PORTION TO TEST?
316
YES
NO
END

Fig. 3

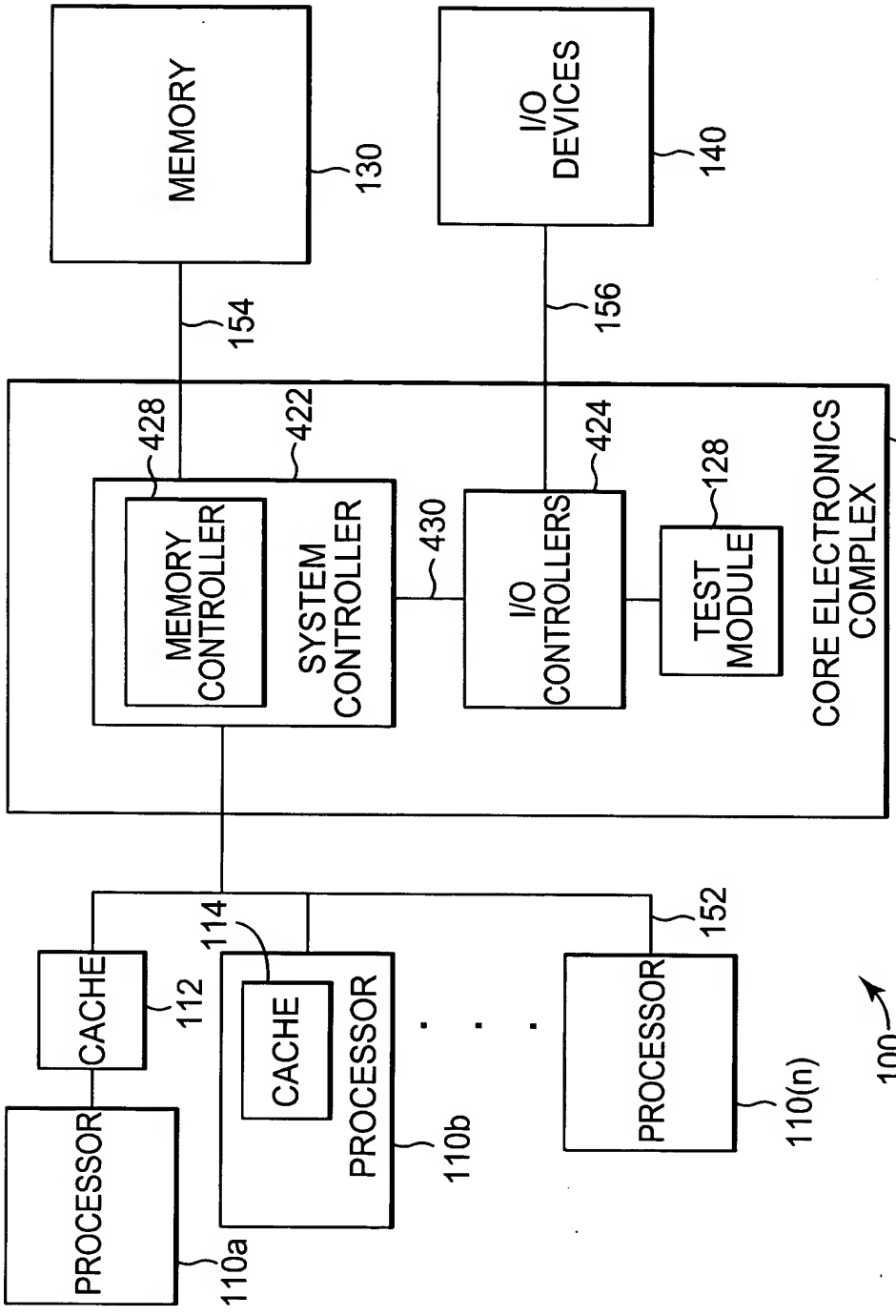
MEMORY
130
I/O DEVICES
140
154
156
428
422
424
128
420
MEMORY CONTROLLER
SYSTEM CONTROLLER
430
I/O CONTROLLERS
TEST MODULE
CORE ELECTRONICS COMPLEX
114
152
CACHE
112
CACHE
PROCESSOR
PROCESSOR
PROCESSOR
110a
110b
110(n)
100

Fig. 4